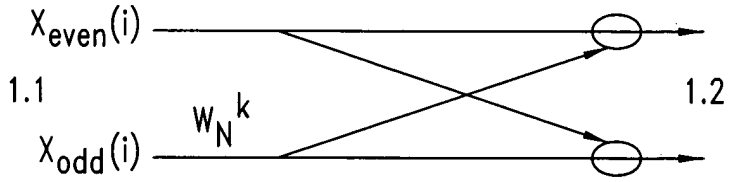

FIG. 1
(Prior Art)

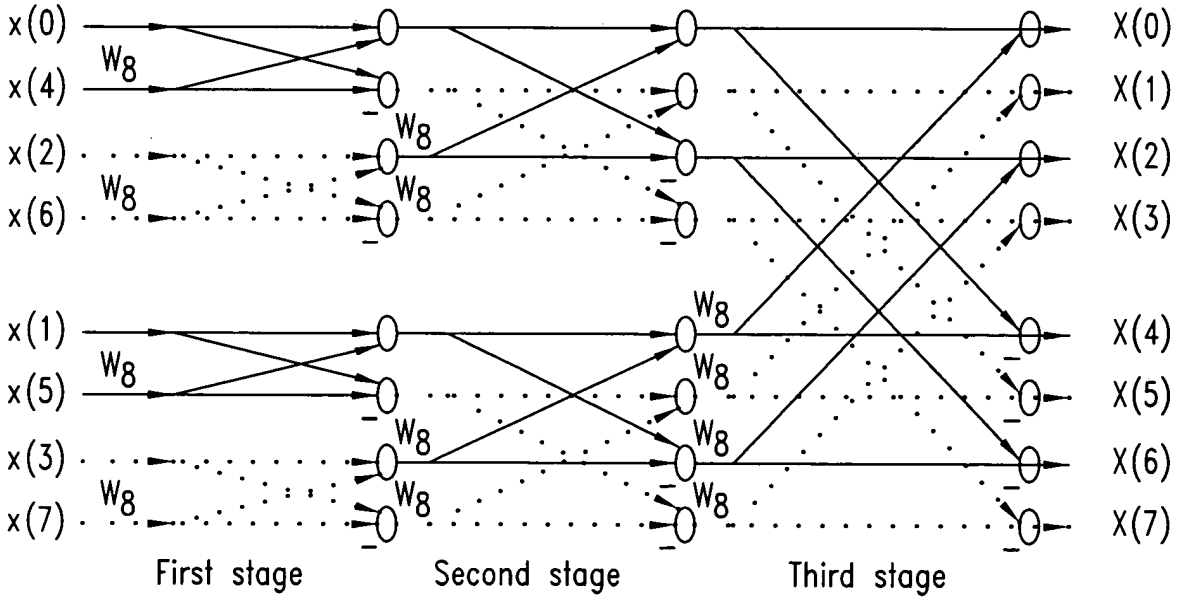

FIG. 2

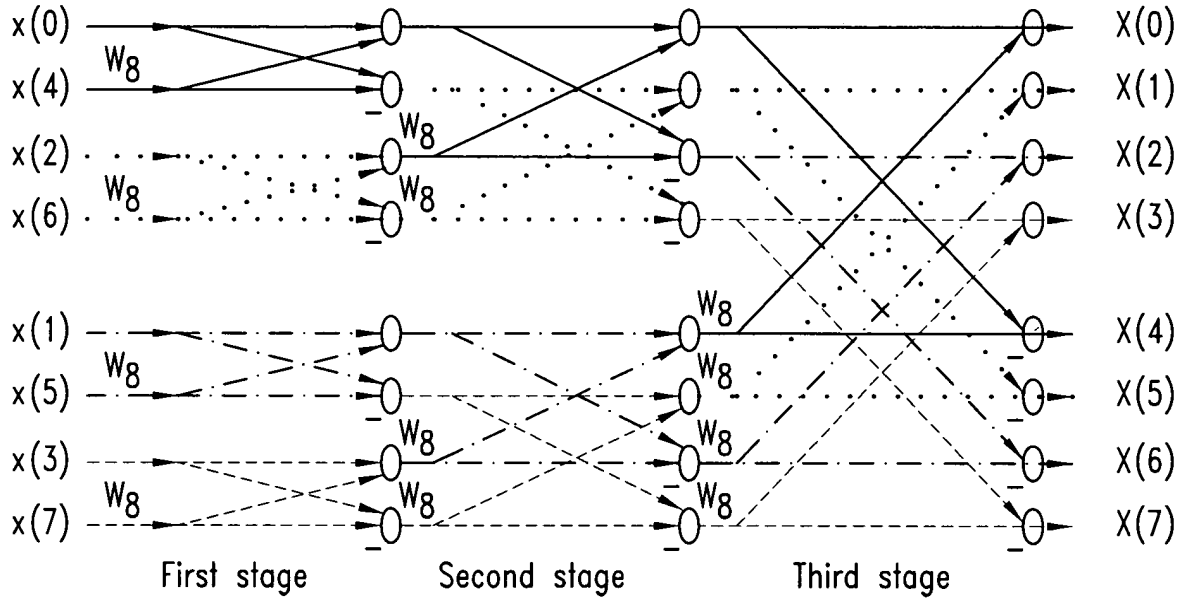
x(0)
x(4)
x(2)
x(6)
x(1)
x(5)
x(3)
x(7)
W8
X(0)
X(1)
X(2)
X(3)
X(4)
X(5)
X(6)
X(7)
First stage
Second stage
Third stage

FIG. 3

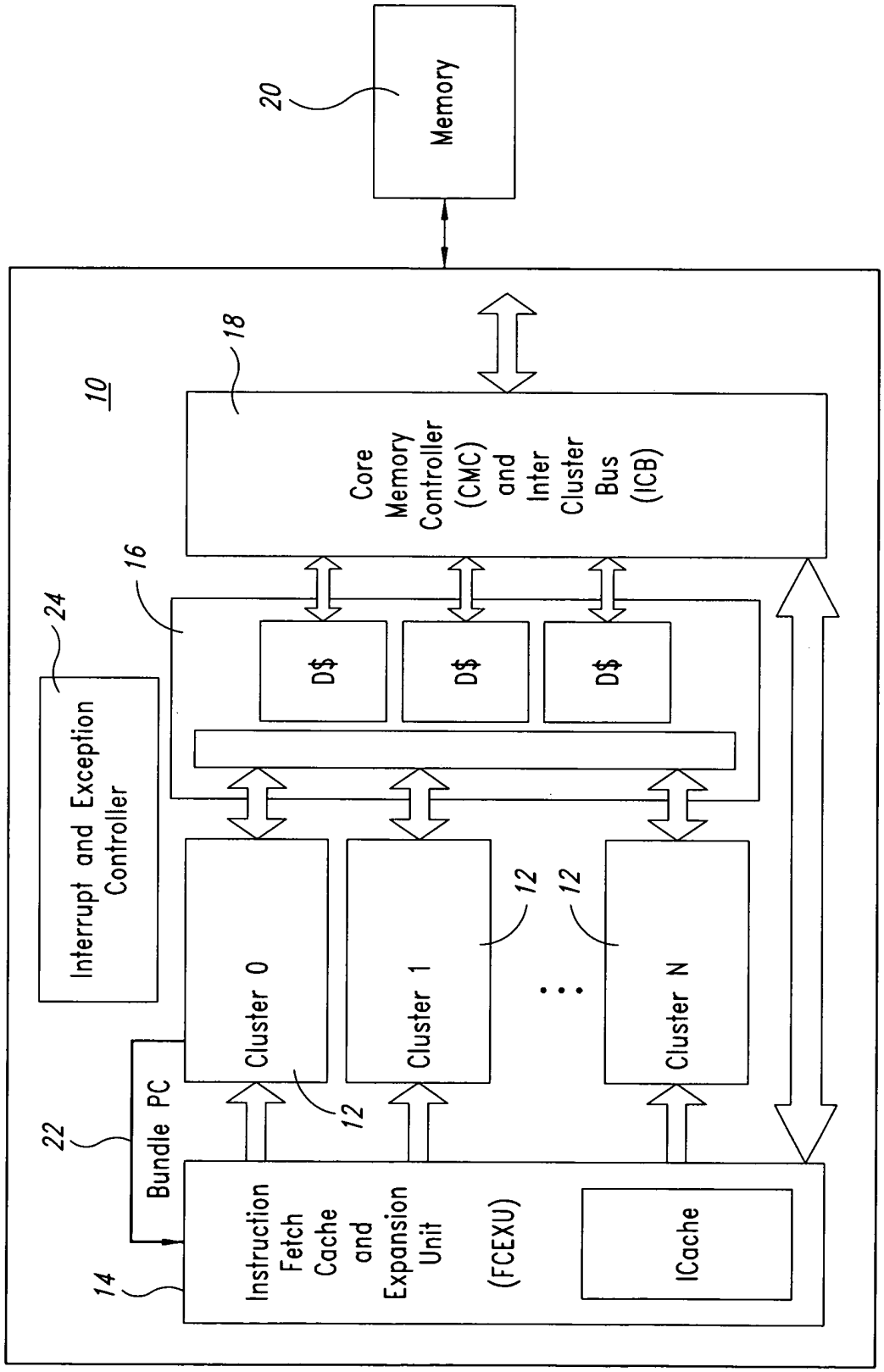
20
Memory
10
18
Core Memory Controller (CMC) and Inter Cluster Bus (ICB)
16
D$
D$
D$
24
Interrupt and Exception Controller
Cluster 0
Cluster 1
Cluster N
12
12
12
22
Bundle PC
14
Instruction Fetch Cache and Expansion Unit (FCEXU)
ICache

FIG. 4

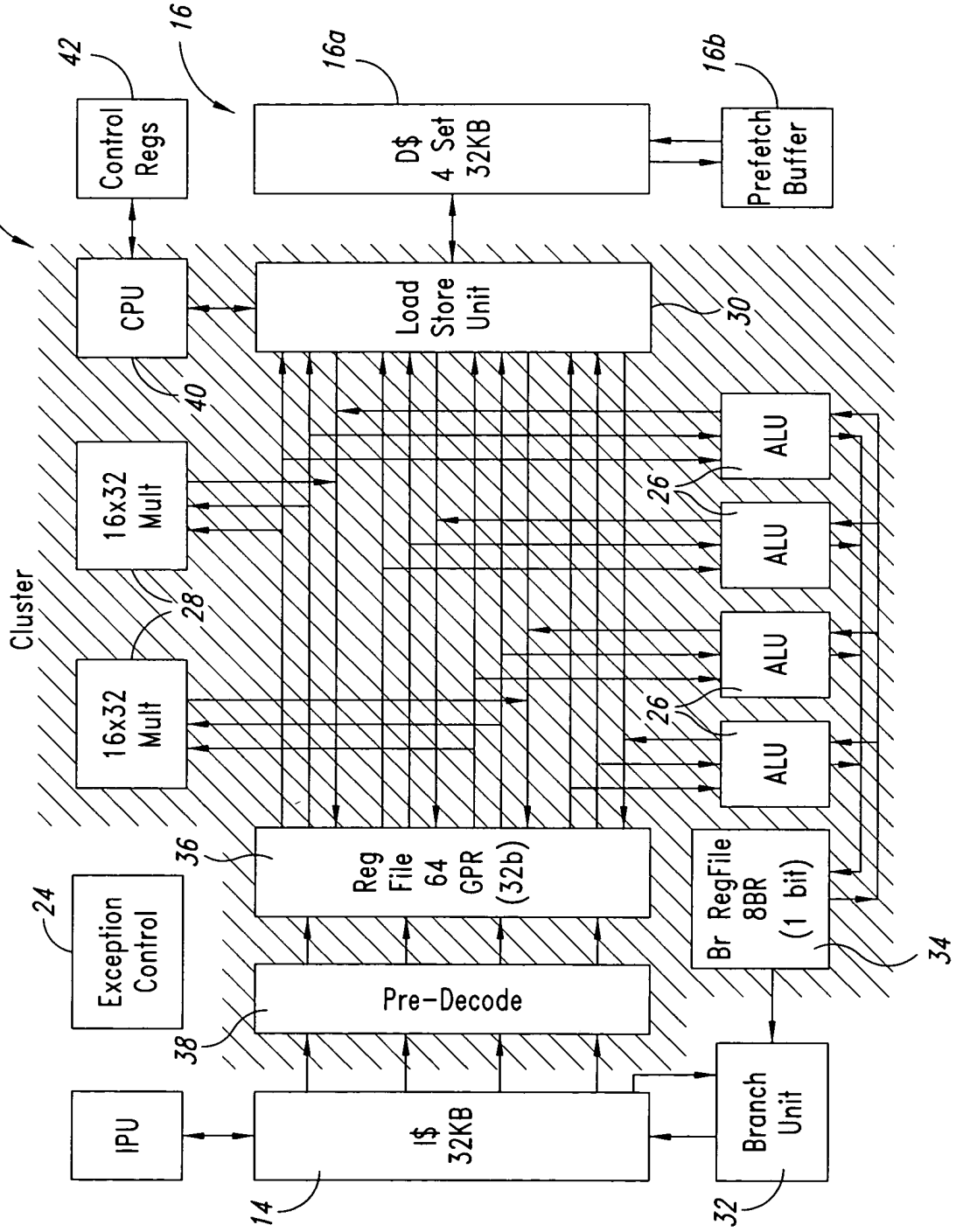
12
42
Control Regs
16
16a
D$ 4 Set 32KB
16b
Prefetch Buffer
CPU
Load Store Unit
30
40
16x32 Mult
16x32 Mult
28
Cluster
ALU
ALU
ALU
ALU
26
26
36
Reg File 64 GPR (32b)
Br RegFile 8BR (1 bit)
34
24
Exception Control
Pre-Decode
38
IPU
I$ 32KB
14
Branch Unit
32

FIG. 5

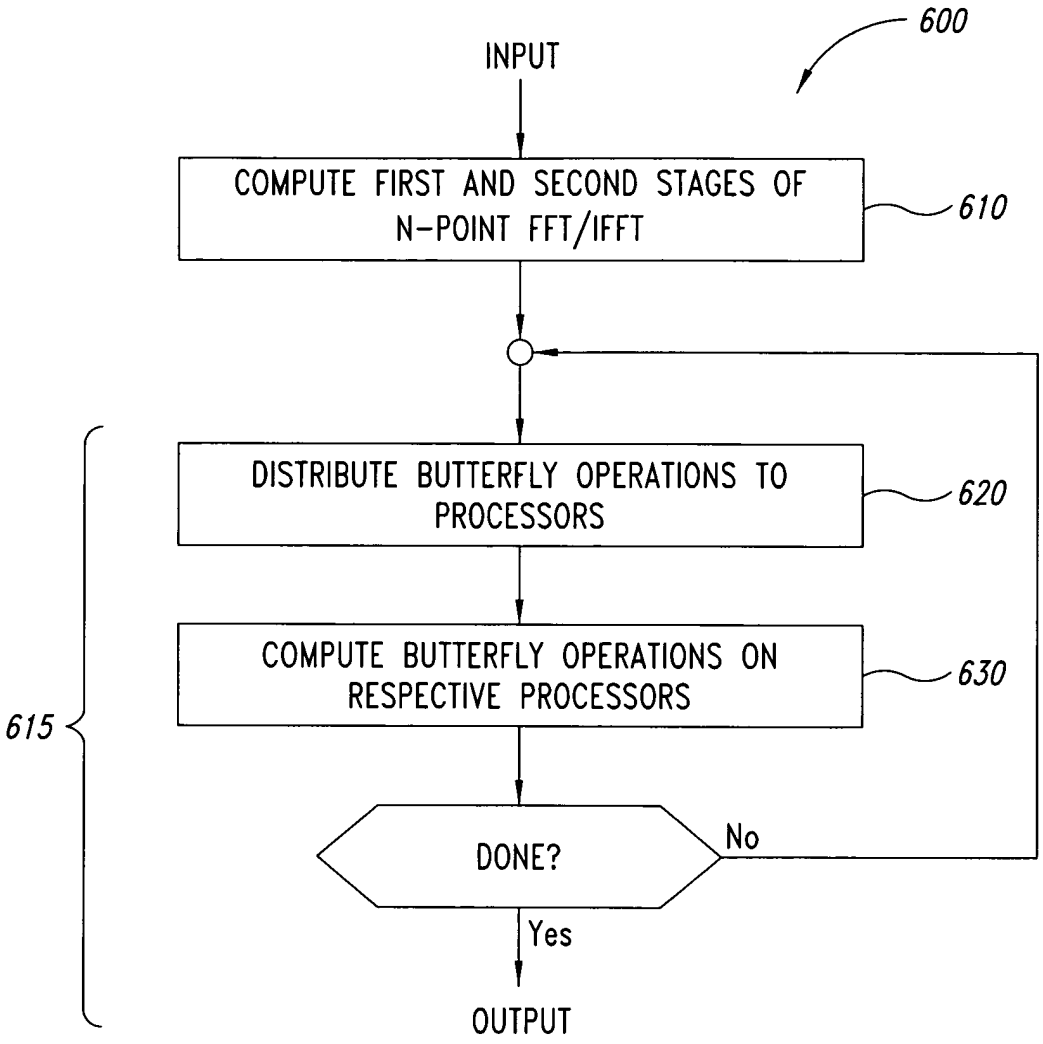
600
INPUT
COMPUTE FIRST AND SECOND STAGES OF N-POINT FFT/IFFT
610
DISTRIBUTE BUTTERFLY OPERATIONS TO PROCESSORS
620
COMPUTE BUTTERFLY OPERATIONS ON RESPECTIVE PROCESSORS
630
615
DONE?
No
Yes
OUTPUT

FIG. 6